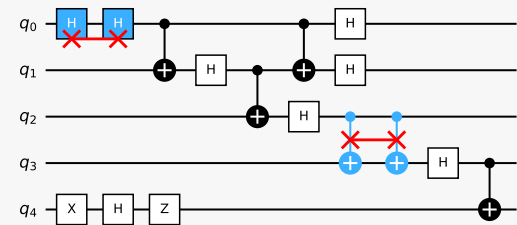
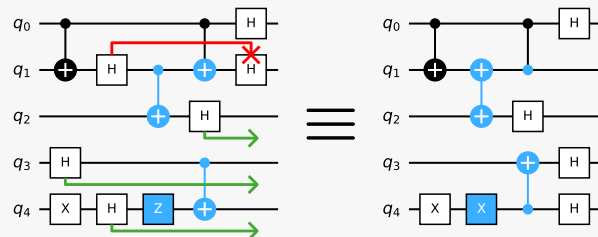


(1) Program circuit

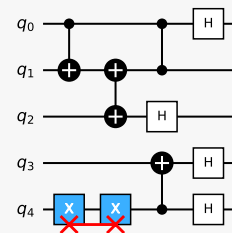
(1a) Gate cancellation



(1b) Hadamard commutation



(1c) Gate cancellation

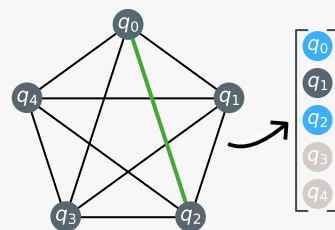


(2) Logical circuit

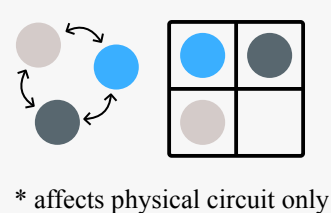
(2a) Score matrix through gate merging

	0	1	2	3
0	$(s_{00}^{(1)}, s_{00}^{(2)})$			
1	$(s_{10}^{(1)}, s_{10}^{(2)})$	$(s_{11}^{(1)}, s_{11}^{(2)})$		
2	$(s_{20}^{(1)}, s_{20}^{(2)})$	$(s_{21}^{(1)}, s_{21}^{(2)})$	$(s_{22}^{(1)}, s_{22}^{(2)})$	
3	$(s_{30}^{(1)}, s_{30}^{(2)})$	$(s_{31}^{(1)}, s_{31}^{(2)})$	$(s_{32}^{(1)}, s_{32}^{(2)})$	$(s_{33}^{(1)}, s_{33}^{(2)})$

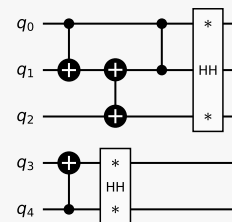
(2b) Pack qubits



(2c) Remap to grid

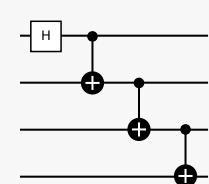


(2d) Rewrite circuit

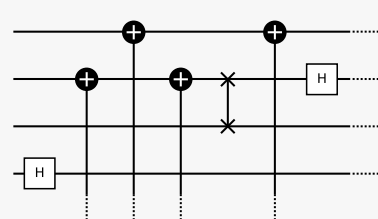


(3) Physical circuit

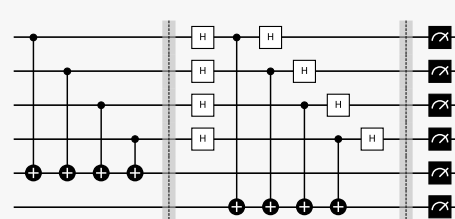
(3a) Encoding



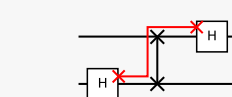
(3b) Translate logical gates



(3c) Decoding and measurement



(3d) Gate cancellation



(4) Output circuit